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REMARKS

I. Introduction

These amendments and remarks are in response to the Non-Final Office Action mailed April 20, 2004 in the above-captioned application. Claims 1-26 are pending in this application. Claims 14 and 15 were amended in a preliminary amendment filed June 30, 2003. Claims 1-20 have been allowed. Claims 21-26 have been rejected.

The specification has been amended in accordance with the Examiner's suggestions to add references for the symbols listed in the figures. Claims 17, 19, 21, 25 and 26 have been amended only to correct typographical errors; no change in the scope of those claims is intended. No new matter has been added in the amendments.

II. Examiner's Objections

The Examiner objected to the specification for the following formalities: (1) on page 32, line 5, "Fi" should be "Fig."; and (2) on page 36, line 11, "Inv41" should be "INV41". In response, Applicants have amended the specification to correct both of these typographical errors as suggested by the Examiner.

The Examiner objected to the drawings as failing to comply with 37 CFR § 1.84(p)(5) because the drawings including the reference signs not mentioned in the description. The reference signs objected to are identified by figure below. Applicants have amended the drawings and/or the specification in response to each objection as summarized below. Support for the amendments to the specification may be found in the corresponding figures or within the specification as discussed below.

Fig. 2 – B/L, W/L, and P/L: Applicants submit herewith a replacement drawing sheet wherein "B/L," "W/L," and "P/L" have been replaced with "BL," "WL," and "PL," respectively.

Fig. 3a – CEB, SEN, ACTIVE and PERCHARGE: Applicants submit herewith a replacement drawing sheet wherein the uppercase letters in "ACTIVE" and "PRECHARGE" have been replaced by lowercase letters. The specification has been amended above to replace "CSB" with "CEB" to correct a typographical error, and to add a description of "SEN" consistent with the description mentioned at page 4, line 23 of the specification.

Fig. 3b - CEB, SEN, DOUT, ACTIVE and PRECHARGE: Applicants submit herewith a replacement drawing sheet wherein the uppercase letters in ACTIVE and PRECHARGE have been replaced by lowercase letters. The specification has been amended above to replace "CSB" with "CEB" to correct a typographical error, and to add a description for "DOUT." Applicants note that "SEN" is mentioned at page 4, line 23 of the specification.

Fig. 10 - CEB, /WE, SBSW1, SBPD, MBLC, MBPUC, and CSN: The specification has been amended to add descriptions of components "CEB," "/WE," "MBLC," "MBPUC," and "CSN." Applicants note that "SBSW1" is mentioned at page 18, line 7 of the specification and "SBPD" is disclosed at page 16, line 17 of the specification, so amendments are not required with respect to these references.

Fig. 11 - CEB, /WE, DOUT, SBSW1, SBPD, MBLC, MBPUC, and CSN: The specification has been amended above to add descriptions of components "CEB," "/WE," "DOUT," "MBLC," and "CSN." Applicants note that "SBSW1" is mentioned at page 21, line 7 of the specification, "SBPD" is mentioned at page 19, line 12 of the specification, and

"MBPUC" is mentioned at page 20, line 5 of the specification, so amendments are not required with respect to these references.

Fig. 12 - 210 and 310: Applicants submit herewith a Replacement Sheet drawing wherein the reference numerals "210" and "21N" have been replaced with "21", and "310" has been replaced with "31".

Fig. 13 - 210 and 310: Applicants submit herewith a Replacement Sheet drawing wherein the reference numerals "210" and "21N" have been replaced with "21", and "310" has been replaced with "31".

Fig. 14 - 150 and WL0: Applicants submit herewith a Replacement Sheet drawing wherein the reference numerals "150", "WL0", "15N", and "WLN" have been replaced with "15", "WL<0>", "15", and "WL<n>".

Fig. 15 - DEC10, DEC20, SBL, and VCC+VPP-Vtn: Applicants submit herewith a Replacement Sheet drawing wherein "SBL" and "SBPU" have been deleted. "WL" and "VCC+VPP-Vtn" have been replaced with "WL<0>" and "VPP", respectively, to be consistent with the specification. The specification has been amended above to add descriptions for "DEC10" and "DEC20."

Fig. 16 - 160 and PL0: Applicants submit herewith a Replacement Sheet drawing wherein "160", "PL0", "16N", and "PLN" have been replaced with "16", "PL<0>", "16", and "PL<n>", respectively.

Fig. 17 - DEC10, DEC20, and VCC+VPP-Vtn: Applicants submit herewith a Replacement Sheet drawing wherein "SBL" and "SBPU" have been deleted. "PL" and "VCC+VPP-Vtn" have been replaced with "PL<0>" and "VPP", respectively, to be consistent with the specification. The specification has been amended above to add a description for "DEC10" and "DEC20."

Fig. 18 - EN0. Applicants note that EN0 is mentioned at page 29, lines 8-10 of the specification, so amendment is not required with respect to this reference.

Fig. 21 - n+ and P SUBSTRATE. Applicants submit herewith a Replacement Sheet drawing wherein "P SUBSTRATE" has been replaced with "P type substrate." Applicants have amended the specification above to refer to "n+."

Fig. 24 - CEBEN and ATD. Applicants have amended the specification above to refer to "CEBEN" and "ATD" consistent with the figure.

III. Examiner's Rejection Under 35 U.S.C. § 102

The Examiner rejected claims 21-26 under 35 U.S.C. § 102 as being anticipated by Fukumoto (U.S. Patent No. 6,370,058).

Applicants respectfully traverse this rejection because the Fukumoto reference does not disclose each and every element of the claims 21-26 as described below.

a) Memory Cell Array

Fukumoto teaches a memory cell array having a conventional structure of a single bitline. In contrast, the memory cell array of the present invention comprises a plurality of sub-memory cell arrays having a systematic bitline structure of a main bitline and a sub bitline. Additionally, the systematic bit line structure disclosed in the present invention is not taught by Fukumoto.

b) Row Address Latch Circuit

The row address latch taught in Fukumoto receives and latches just row addresses. In contrast, the address latch of the present invention receives all addresses irrespective of row or column.

c) Address Transition Detecting Circuit

The address transition detecting circuit of Fukumoto's invention performs a read operation in synchronization with the transition of address (see col. 12, lines 67 to col. 13, line 4). Thus, Fukumoto teaches a volatile mode/address transition detection (ATD) timing generation circuit and does not teach outputting an address detection signal.. In contrast, the address transition detecting circuit of the present invention detects the transition time of an address outputted from an address latch in response to a clock enable signal.

d) Address Buffer Circuit

The address buffer circuit of the present invention buffers an address pad signal inputted through an address pad and outputs it to an address latch. This structure is not disclosed in Fukumoto which neither teaches nor suggests the connectivity of an address buffer and a row address latch circuit illustrated in Fig. 10. Accordingly, the address buffer of the present invention is different from that taught in Fukumoto.

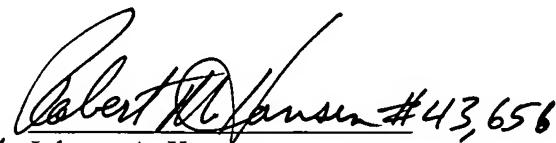
Because Fukumoto does not teach all of the elements of claims 21-26, Applicants consider claims 21-26 to be allowable and respectfully request withdraw of the rejections under 35 U.S.C. §102(b).

IV. Conclusion

In view of the above amendments and remarks, withdrawal of the objections to the specification and drawings and rejections of claims 21-26 under 35 U.S.C. § 102 are respectfully requested. Applicants believe that all claims are now in condition for allowance, and request that a timely Notice of Allowance be issued in this application. Should the Examiner have any questions, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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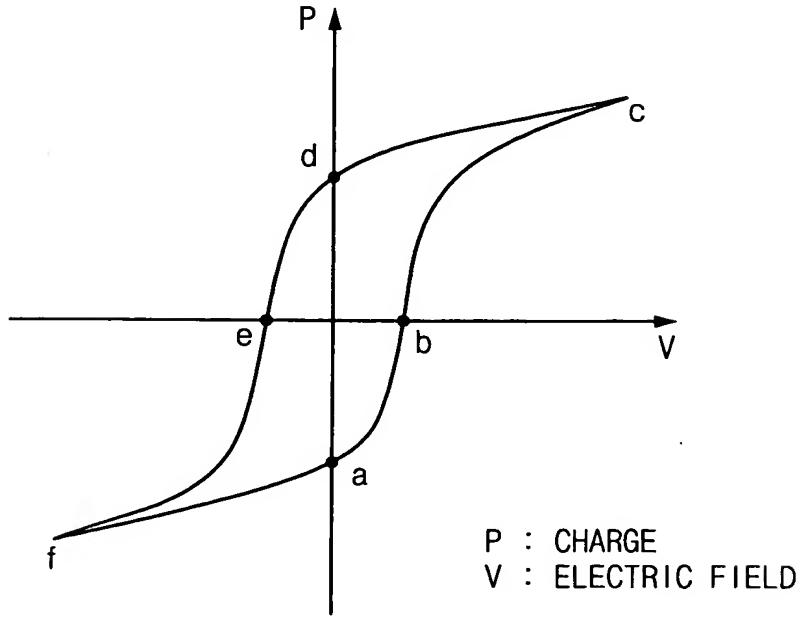


Fig.1
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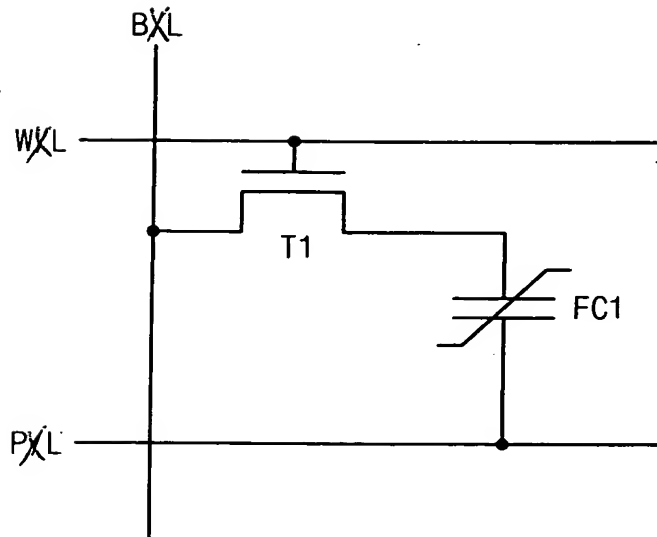


Fig.2
<Prior Art>

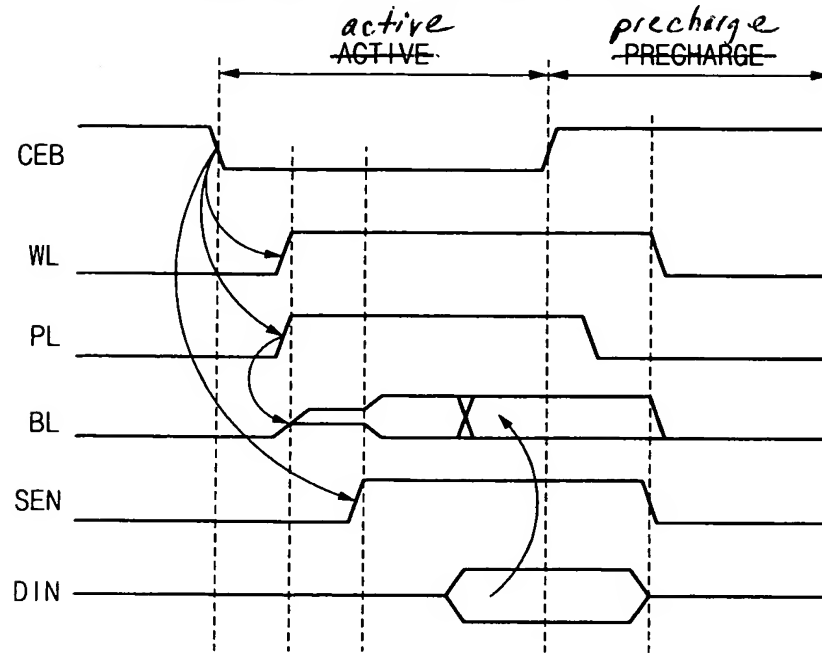


Fig.3a
<Prior Art>

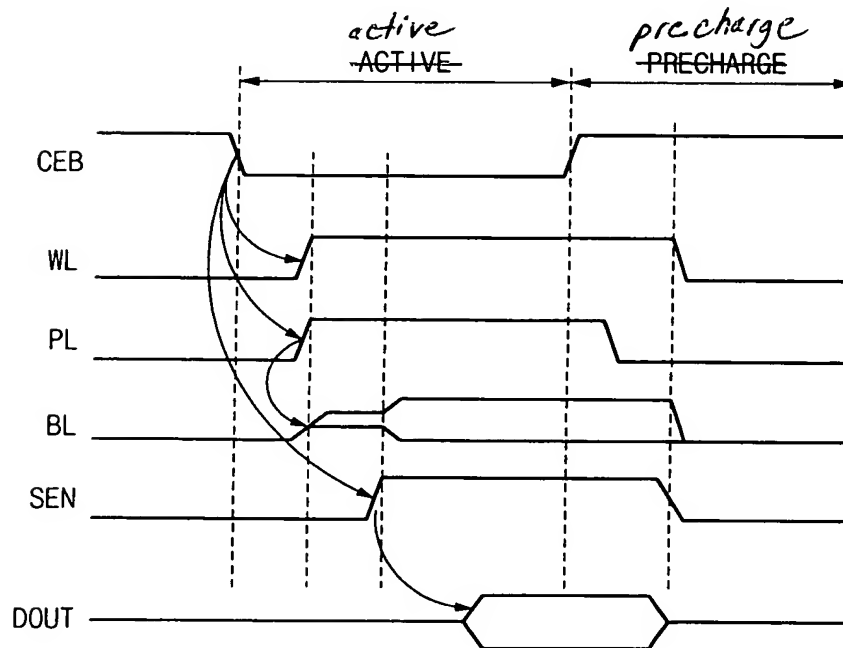


Fig.3b
<Prior Art>

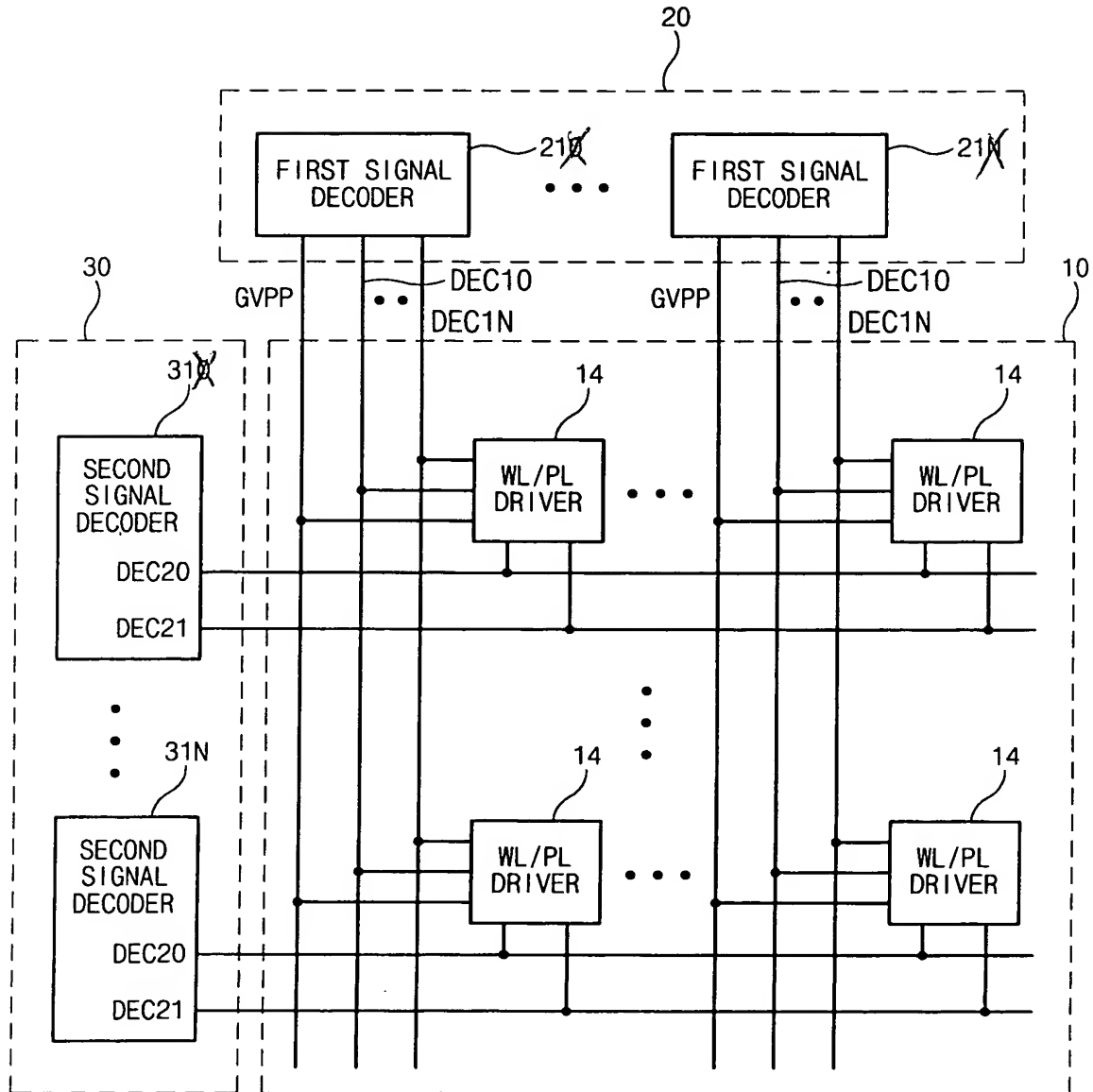


Fig.12

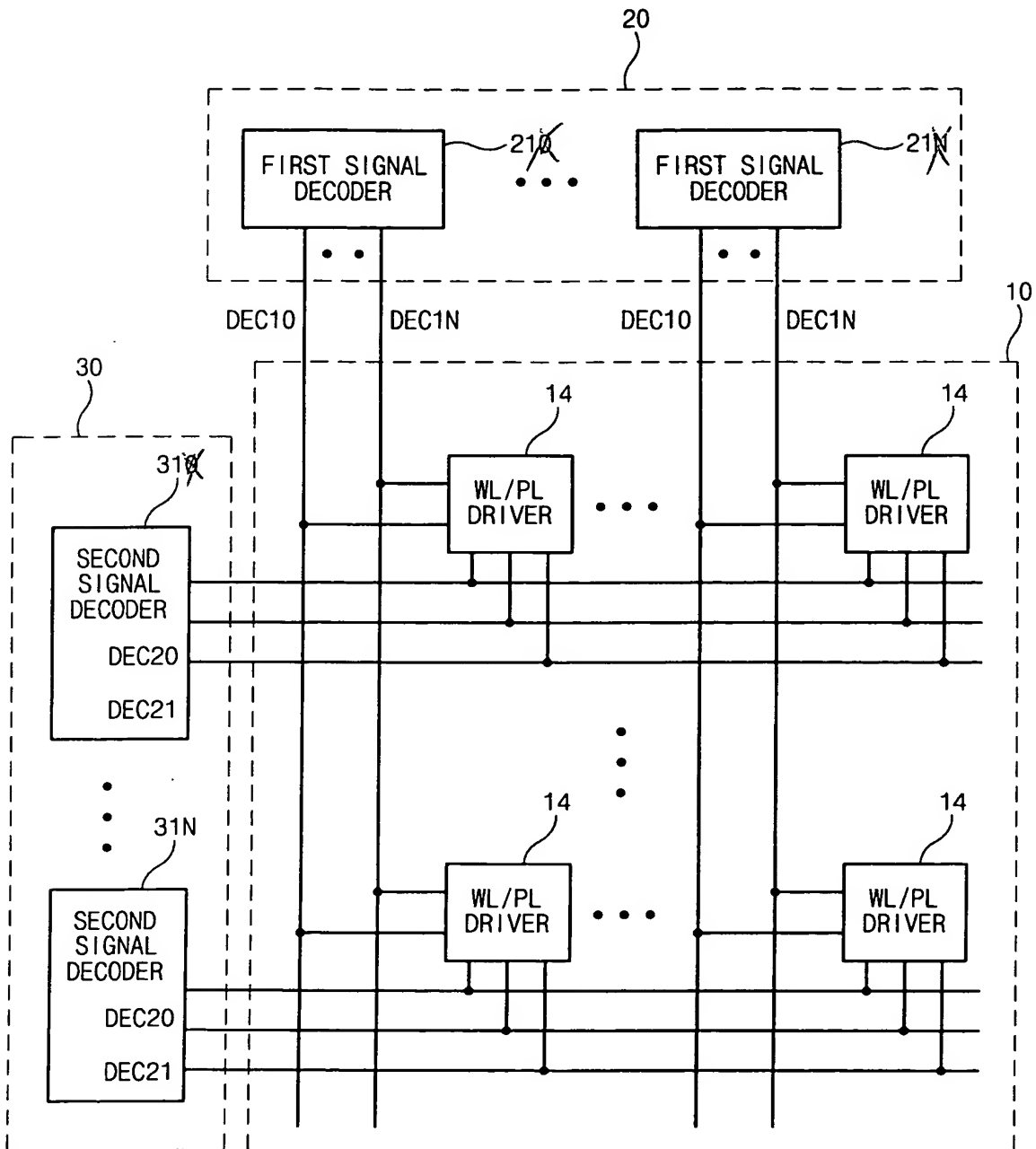


Fig.13

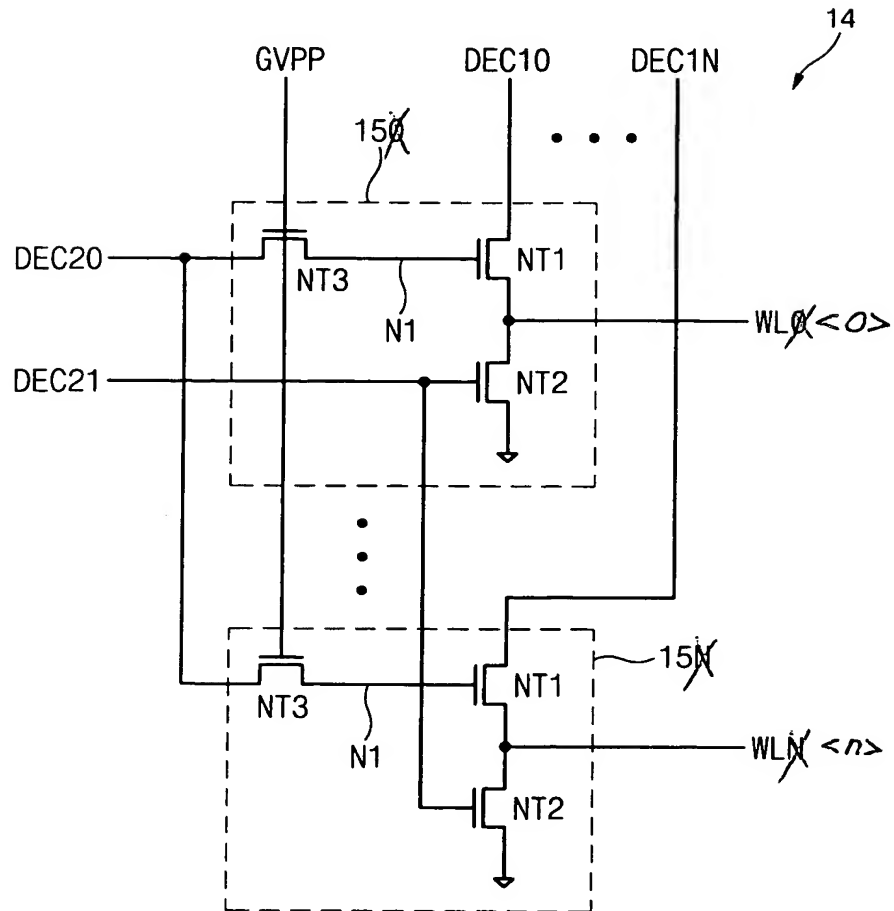


Fig.14

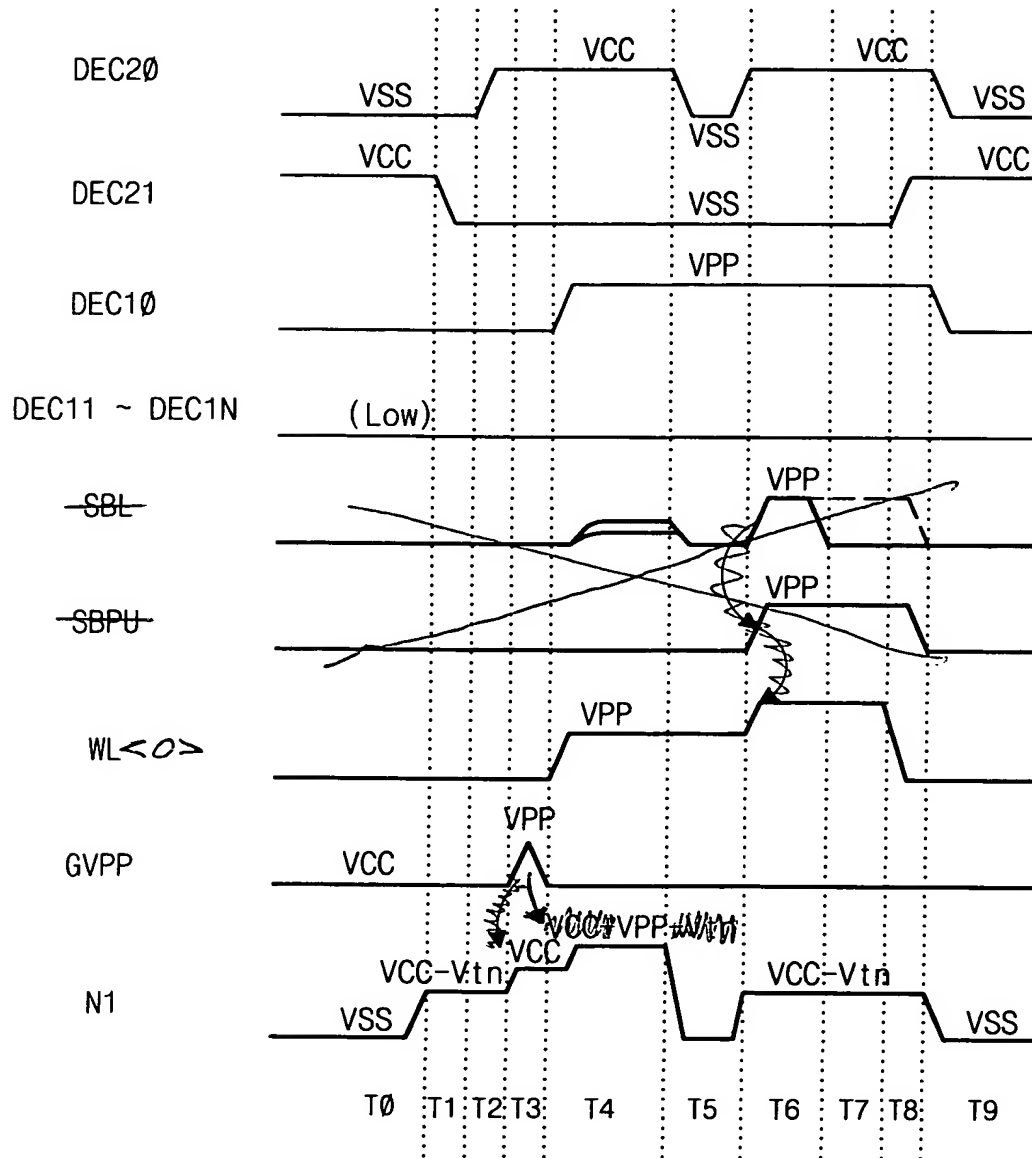


Fig.15

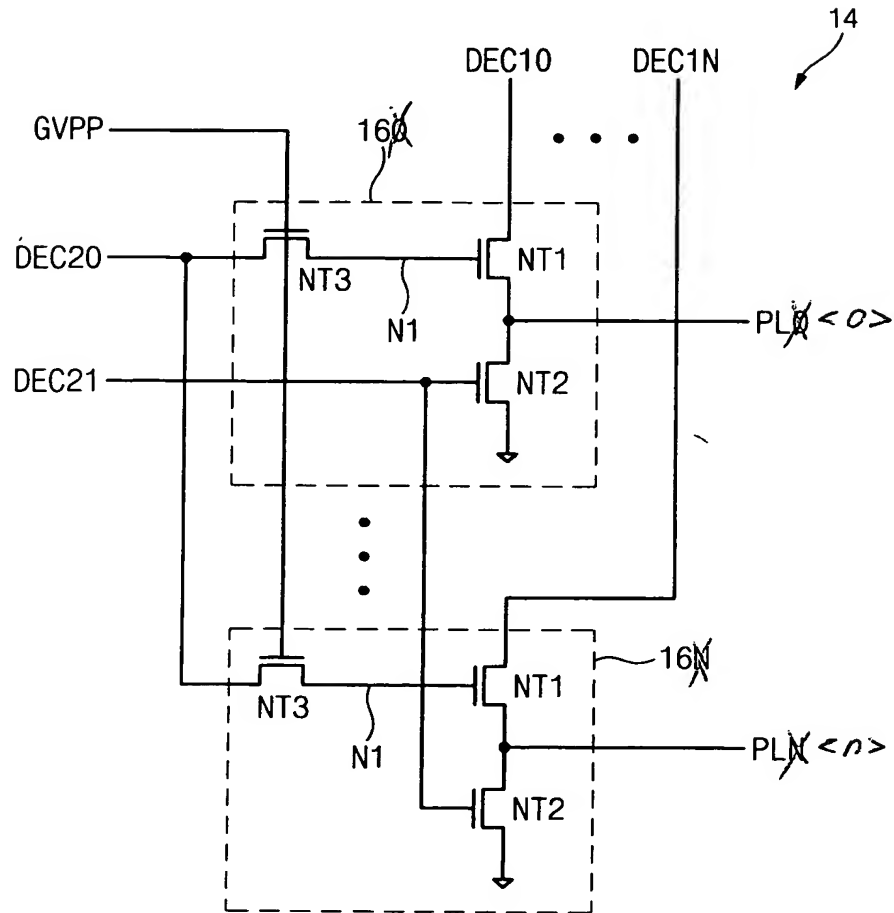


Fig.16

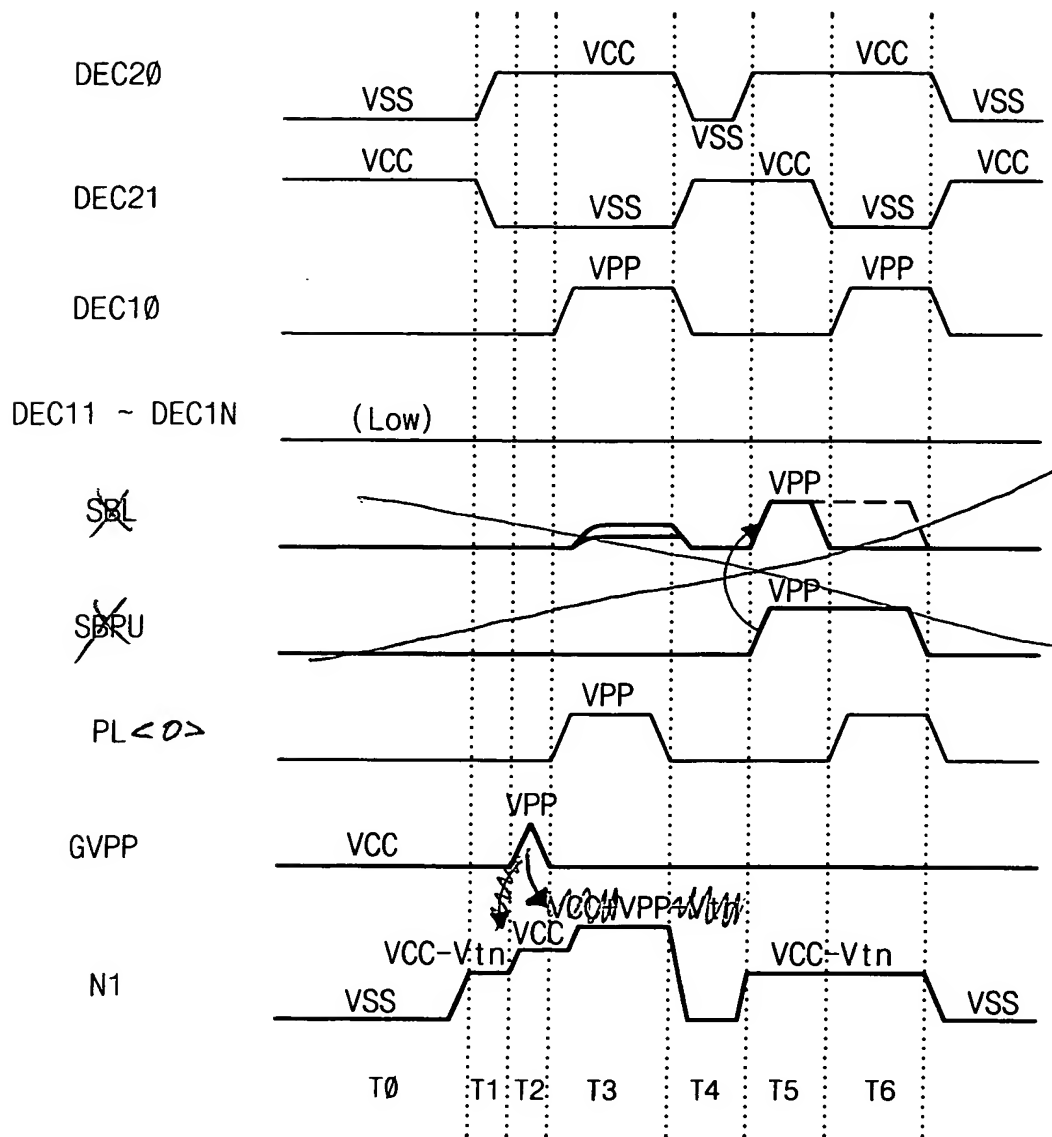


Fig.17

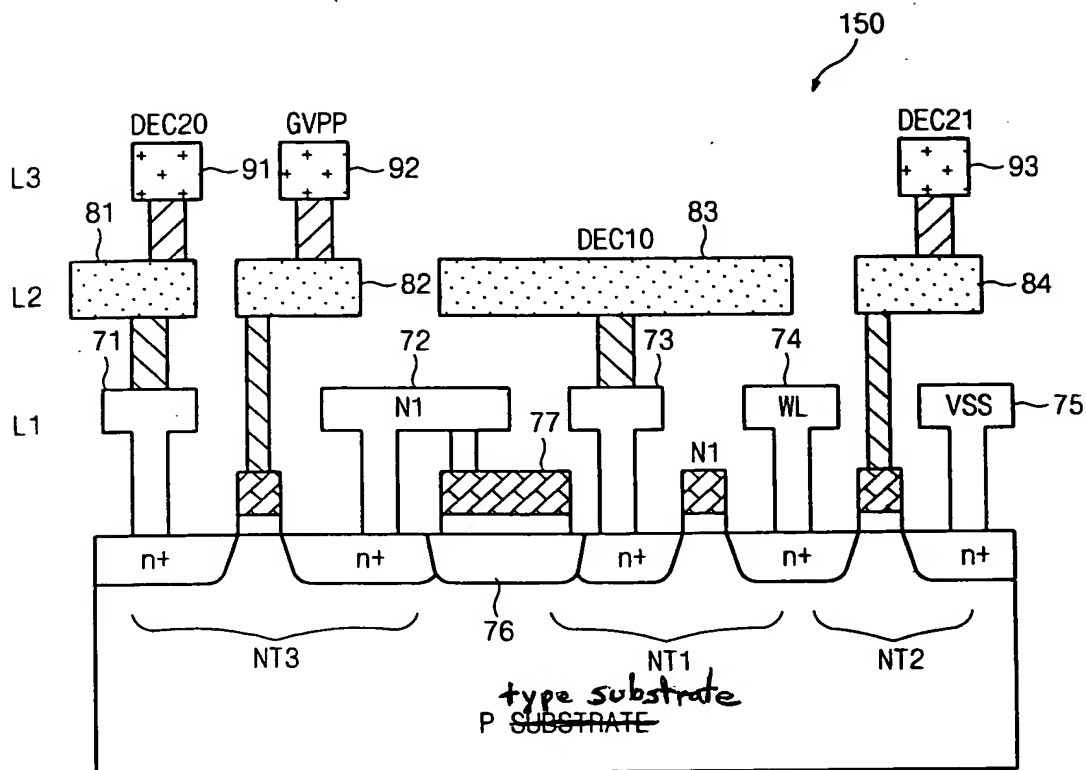


Fig.21